Introduction to Digital Logic

EECS/CSE 31L

**Assignment 1: 2-Bit Encoder**

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**1 Block Description**

This block is deigned to take in an enable and 2 inputs and encode it into 1 output

**2 Input/Output Port Description**

|  |  |  |  |
| --- | --- | --- | --- |
| Port name | Port size | Port Type | Description |
| Enable | 1 | IN | Enable the operation to occur |
| Input0 | 1 | IN | Gets the first operand |
| Input1 | 1 | IN | Gets the second operand |
| output | 1 | OUT | The operation result |

**3 Design Schematics**

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| Enable | In\_1 | In\_0 | F |
| 0 | X | X | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**Boolean Expressions:**

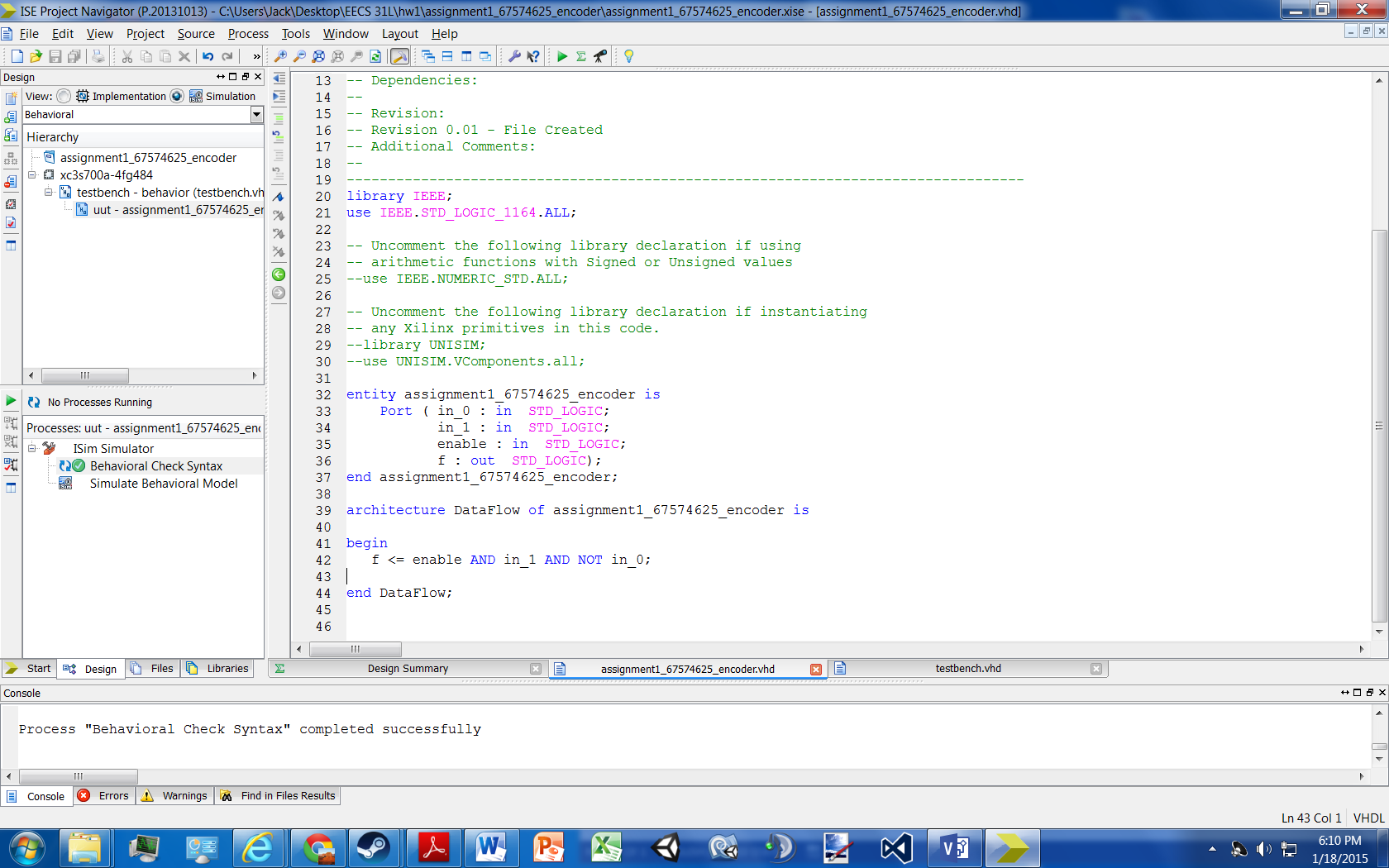
F = (Enable)(In\_1)(In\_0’)

**Gate Representation:**

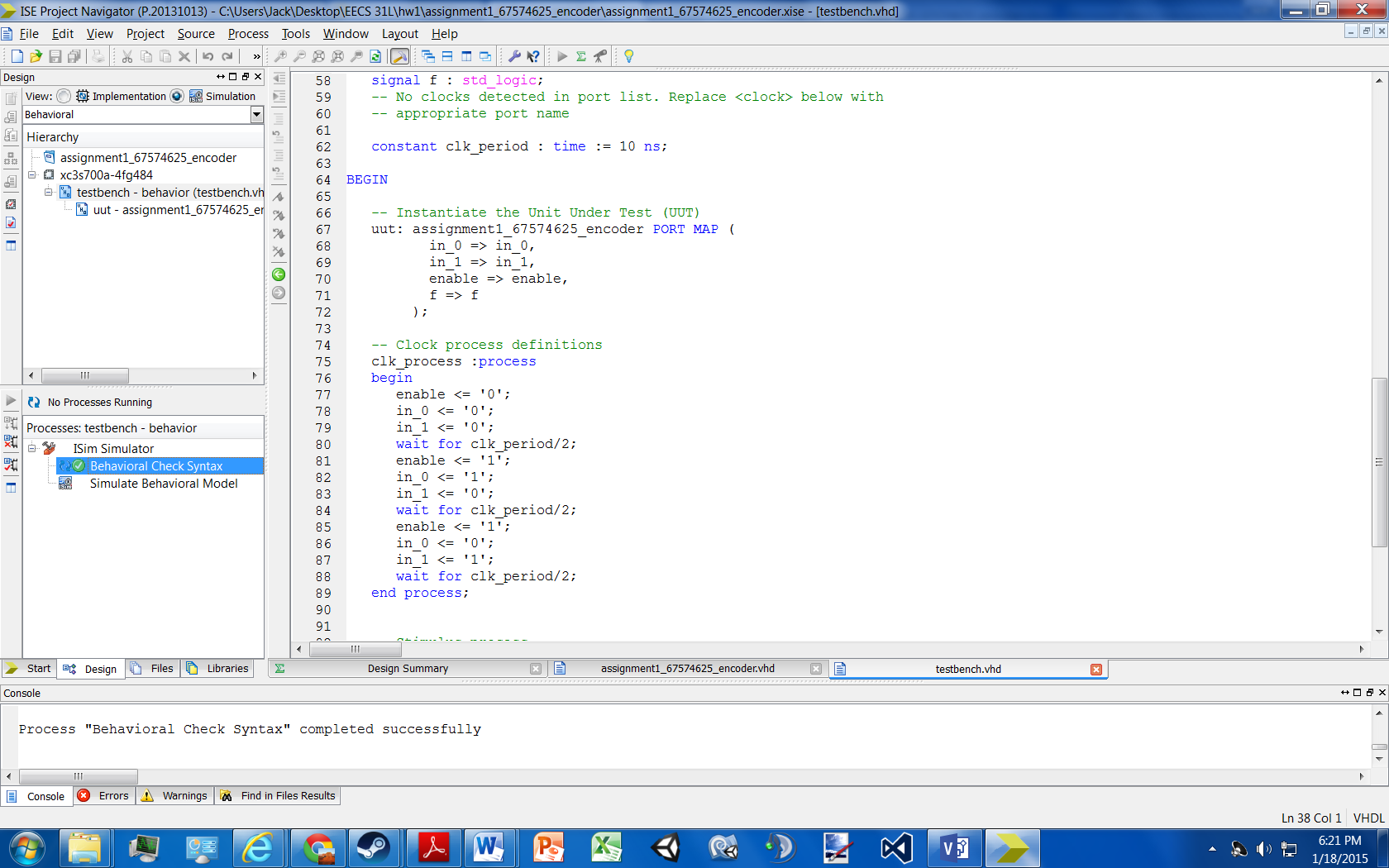


**4 Compilation**

Encoder compiled



Testbench compiled



**5 Elaboration**

**Assumptions:**

* while enable = ‘0’ , in\_0 and in\_1 can be either ‘0’ or ‘1’ (not shown in waveform)
* encoders do not use input combinations “00” or “11” while enabled

**Errors:**

* No errors occurred while coding

**Simulation Log:**

Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...

Running fuse...

Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_encoder/testbench\_isim\_beh.exe} -prj {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_encoder/testbench\_beh.prj} work.testbench {}

Running: C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_encoder/testbench\_isim\_beh.exe -prj C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_encoder/testbench\_beh.prj work.testbench

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 4

Turning on mult-threading, number of parallel sub-compilation jobs: 8

Determining compilation order of HDL files

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_encoder/assignment1\_67574625\_encoder.vhd" into library work

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_encoder/testbench.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std\_logic\_1164

Compiling architecture dataflow of entity assignment1\_67574625\_encoder [assignment1\_67574625\_encoder\_def...]

Compiling architecture behavior of entity testbench

Time Resolution for simulation is 1ps.

Compiled 5 VHDL Units

Built simulation executable C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_encoder/testbench\_isim\_beh.exe

Fuse Memory Usage: 29820 KB

Fuse CPU Usage: 420 ms

Launching ISim simulation engine GUI...

"C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_encoder/testbench\_isim\_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_encoder/testbench\_isim\_beh.wdb"

ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

**6 Waveform**

